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AN EXPERIMENTAL STUDY OF
VOICE COMMUNICATION
OVER A BANDLIMITED CHANNEL USING
VARIABLE BIT WIDTH DELTA MODULATION

by

N. Nur Tumok

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Only baseband modulation is applied to the input signal. Since there is no "clock" used during the digitizing process at ne modulator, no bit synchronization is required for signal recovery in the receiver. The modulator is a hybrid design using linear and 3 digital integrated circuits (IC), and the demodulator uses 2 linear ICs. A lowpass filter (LPF) is used to simulate ne channel. The average number of bits sent over the channel is measured with a frequency counter at the output of the nodulator. The minimum bandwidth required for the LPF is determined according to the intelligibility of the recovered nessage.

Measurements indicate an average bit rate required for intelligible voice transmission is in the range of 2 to 4 kilobits per econds (kbps) and between 2 to 5 kbps for music. The channel 3 dB bandwidth required is determined to be 1.5 kHz.

Besides the hardware simplicity, VBWDM provides an option for intelligible digitized voice transmission at very low bit ates without requiring synchronization. Another important feature of the modulator design is that no bits are sent when no ignal is present at the input which saves transmitter power (important for mobile stations) and reduces probability of interept and jamming in military applications.

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An Experimental Study of Voice Communication Over a Bandlimited Channel Using Variable Bit Width Delta Modulation

by

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Lieutenant Junior Grade Turkish Navy
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ABSTRACT

A variable bit width delta modulator (VBWDM) demodulator was designed, built and tested to achieve voice and music communication using a bandlimited channel.

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LIST OF SYMBOLS AND ABBREVIATIONS

A-to-D	Analog-to-Digital
ADC	Analog-to-Digital Converter
BW	Bandwidth
bps	Bits Per Second
CVSDM	Continuously Variable Slope Delta Modulaton
DAC	Digital-to-Analog Converter
D-to-A	Digital-to-Analog
DM	Delta Modulation
dc	Direct Current
e(t)	Error Waveform
f_g	Square Wave Generator Frequency
Hz	Hertz
IC	Integrated Circuit
kbps	Kilobits Per Second
kHz	Kilohertz
k Ω	Kilohm
LPF	Lowpass Filter
Op Amp	Operational Amplifier
Ω	Ohm
TTL	Transistor Transistor Logic
t	Time
VBWDM	Variable Bit Width Delta Modulation
VCO	Voltage Controlled Oscillator
V_{pp}	Peak-to-Peak Voltage
V_{ref}	Voltage Comparator Reference Voltage
x(t)	Analog Input Waveform to Modulator
$\hat{x}$ (t)	Demodulator Output Waveform
y(t)	Digital-to-Analog Converter Output Waveform

I. INTRODUCTION

In a typical digitized voice communication system, the analog voice signal is sampled and the sample values are converted to a digital (usually binary) signal. A voltage representing these digits is transmitted over a communication channel (i.e., phone wire, waveguide, free space). At the receiver the recovered digits are converted back to analog form for reproduction of the voice signal.

Pulse code modulation (PCM) is a well-known method for the analog-to- digital conversion of voice signals. In PCM telephone applications, the standard bit rate is 64 kbps.

An alternative method of analog to digital conversion is delta modulation (DM). DM is much simpler and cheaper than PCM [Ref. 1]. Also, for voice signals, DM offers a bit rate or channel bandwidth reduction capability when compared with PCM, especially in telephone communication systems [Ref. 2: p. 69].

All present DM systems use a clock to generate bits at a fixed rate (16 kbps or 32 kbps). The U.S. military standard is 16 kbps using continuously variable slope delta modulation (CVSDM).

The objective of this research is to construct and operate an unclocked DM. A second objective is to determine the minimum bandwidth required to transmit intelligible speech represented by the variable-width bits.

This report presents the design, characteristics and test results of an unclocked variable bit width delta modulator (VBWDM) as well as a hard limiter type of analog-to-digital converter that are used for digitized voice communication over a bandlimited channel. The channel is simulated by a filter. A block diagram of the experimental setup is shown in Figure 1.

Chapter II presents the background for better understanding of a DM system and the comparison of DM with PCM. A brief discussion of the hardware designs that are realized in this research is also included in this chapter.

Chapter III is focused on VBWDM. Detailed descriptions of design and operation of the hardware blocks that constitute the VBWDM, the channel filter and the receiver subsystem are given in this chapter.

Chapter IV gives the detailed description of the hardware and the operation of the hard limiter type of analog-to-digital converter. Although this design is totally inde-

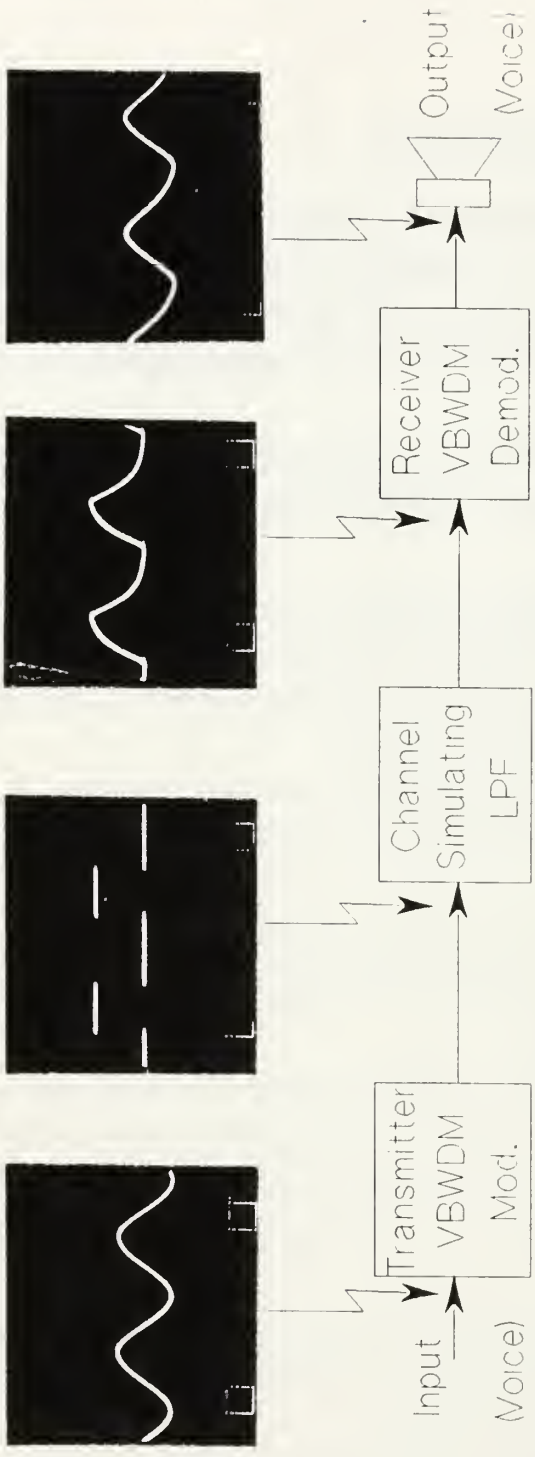


Figure 1. The block diagram of the experimental setup.

pendent from the VBWDM design, the same hardware blocks for the channel simulating filter and for the receiver are used. This enables comparison of the performance of both systems. In both chapters, pictures and diagrams related to the design and operation of the systems are presented.

The results of the research are presented in Chapter V. The conclusions and the recommendations are in Chapter VI. The circuit diagrams are included in the Appendix.

II. BACKGROUND AND DISCUSSION OF DESIGN TYPES

A. BACKGROUND

The idea of coding the human voice into digital pulses was conceived more than four decades ago. Exploitation had to await the ushering in of the transistor era. Various digitizing systems have gradually evolved. [Ref. 2: p. 69]

One method of digitization is to sample the analog signal at regular discrete intervals and code the sample values into binary words. This procedure is called pulse code modulation (PCM). [Ref. 2: p. 69]

Since the difference between adjacent time samples for speech is small, sampling techniques have evolved based on transmitting sample-to-sample differences rather than the actual sample values. Thus the communication task is that of transmitting the difference (the error signal) between the predicted and the actual data sample. For this reason, this class of coder is often called differential pulse code modulator (DPCM). [Ref. 3: pp. 628-629]

The exploitation of signal correlations in DPCM suggests the further possibility of oversampling a signal to increase the adjacent sample correlation and thus to permit the use of a simple quantizing strategy. Delta modulation (DM) is precisely such a scheme. In its original form, the DM coder operates by approximating an input time function by a series of linear segments of constant slope. Such a coder is therefore referred to as a linear delta modulator (LDM). [Ref. 4: p. 621]

A DM system suffer from two types of quantizing error, slope overload distortion and granular noise. Slope overload is said to occur when the step size is too small to follow a steep segment of the input waveform. Granularity on the other hand, refers to a situation where the staircase function hunts around a relatively flat segment of the input function because the step size is too large relative to the local slope characteristics of the input. Therefore, relatively small values of step size accentuate slope overload, while relatively large values of step size increase granularity. [Ref. 4: p. 622]

The step size also determines the peak error when the slope is very small. For example, it is easily verified that, when the input is zero (idle channel condition), the output of the quantizer will be an alternating sequence of 0's and 1's in which case the reconstructed signal at the decoder will alternate about zero (or some constant level)

with peak-to-peak variation of the step size. This latter type of quantization error is also called granular noise. [Ref. 5]

It is therefore clear that the choice of optimum step size that maximizes the mean-square value of the quantizing error in a LDM will be the result of a compromise between slope overload distortion and granular noise. [Ref 6: p. 449]

It is apparent that in DM systems the rate of information is simply equal to the sampling rate. [Ref. 6: p. 446]

A block diagram of a basic DM system is shown in Figure 2. The principal virtue of DM is its simplicity. It may be generated by applying the sampled version of the incoming signal to a modulator that involves a summer, quantizer and accumulator [Ref 6: p. 446].

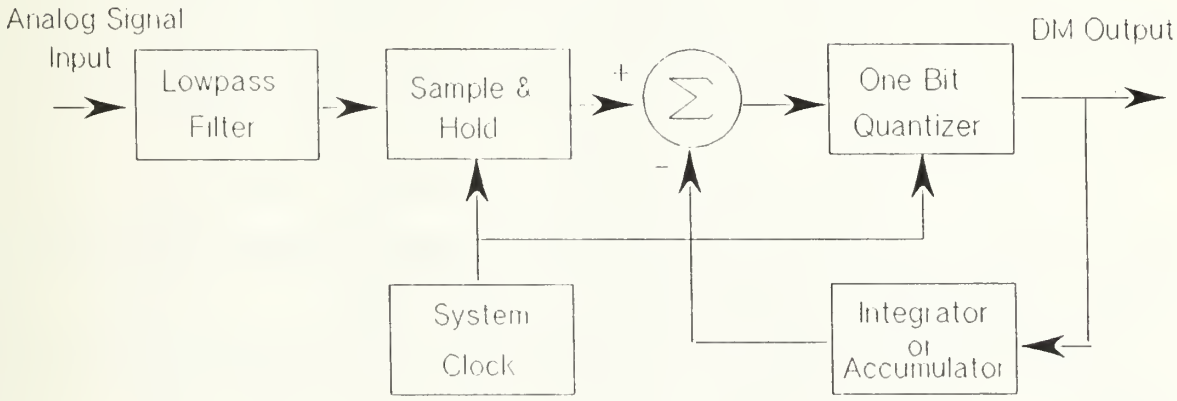


Figure 2. The block diagram of a basic DM.

Important differences between a basic DPCM and a DM networks are the use of a 2-level (1-bit) quantizer in DM and replacement of a general predictor network with a simple integrator which can be regarded as a first-order predictor with prediction coefficient equal to one corresponding to perfect integration (less than one to leaky integration). [Ref. 4: p. 622]

Subjective voice tests and noise measurements have shown that a DM system (linear) operating at 40 kbps is equivalent to a standard PCM system operating with a sampling rate of 8 kHz and 5 bits per sample. At lower bit rates, DM is better than standard PCM (the latter still using 8 kHz sampling and a reduced number of bits per

sample), but at higher bit rates, PCM is superior to DM. The quality of 5-bit PCM is low for most purposes in telephony. For telephone quality voice signals, it has become conventional to use 8-bit PCM. Equivalent voice quality with DM can be obtained by using bit rates much larger than 64 kbps [Ref. 6: pp. 450-451]. The military standard for digitized voice communication is 16 kbps using continuously variable slope delta modulation (CVSDM).

The use of DM is therefore recommended only in certain circumstances: (1) if it is necessary to reduce the bit rate below 40 kbps and limited voice quality is tolerable, or (2) if extreme circuit simplicity is of over-riding importance and the accompanying use of a high bit rate is acceptable. [Ref. 6: p. 450]

B. DISCUSSION OF THE DESIGN TYPES

Present DM systems use a clock to generate bits at fixed rates (16 kbps or 32 kbps). The system clock that runs at a fixed rate usually determines the sampling rate. This procedure also requires lowpass filtering of the input signal (before sampling) to remove all frequency components exceeding one-half of the sampling rate. This filter is referred to as an anti-aliasing filter.

This research investigates experimentally an unclocked DM. The bits have variable width. Therefore bit rate is not a constant quantity. Because of these features, this type of DM is called variable bit width delta modulator (VBWDM).

The first VBWDM hardware design consisted of three main elements: a differential amplifier, a hard limiter (quantizing element) and an analog integrator (leaky) at the feedback loop. The block diagram of this design is shown in Figure 3.

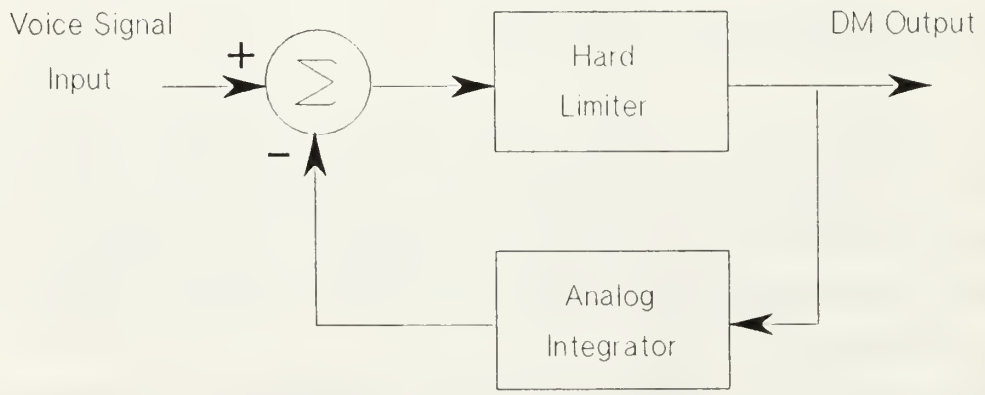


Figure 3. Block diagram of the first VBWDM design.

The result was unsatisfactory because of oscillation inside the loop due to the high gain of the hard limiter. A second design replaced the analog integrator in the feedback loop with a digital integrator to eliminate the oscillation. The block diagram is shown in Figure 4. Stable operation is achieved, but the bit rate is high because of the granular noise.

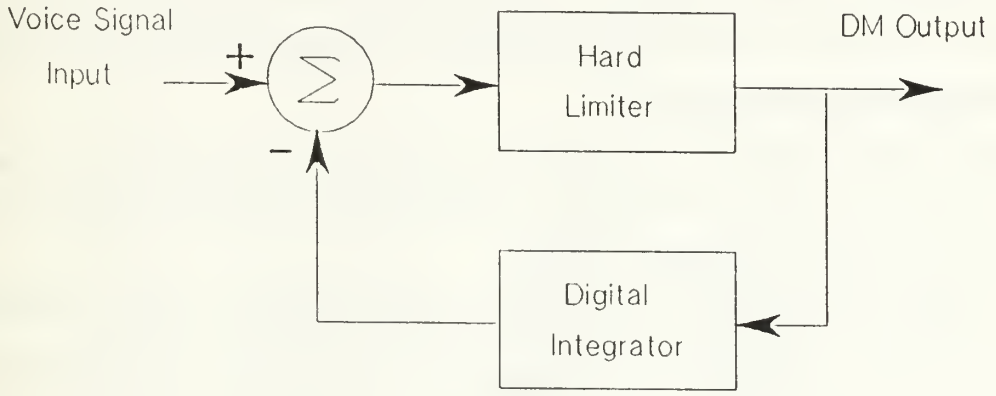


Figure 4. Block diagram of the second VBWDM design.

As a modification to the second VBWDM design to reduce the granular noise, a bit rate reduction circuit is added to the output of the hard limiter. Figure 5 shows the final version of the VBWDM design with this modification. In Chapter III, the design of this VBWDM shown in Figure 5 is presented in detail. An open-loop type of variable bit width ADC (modified hard limiter) was also built and tested as a part of this research. This design is treated in Chapter IV.

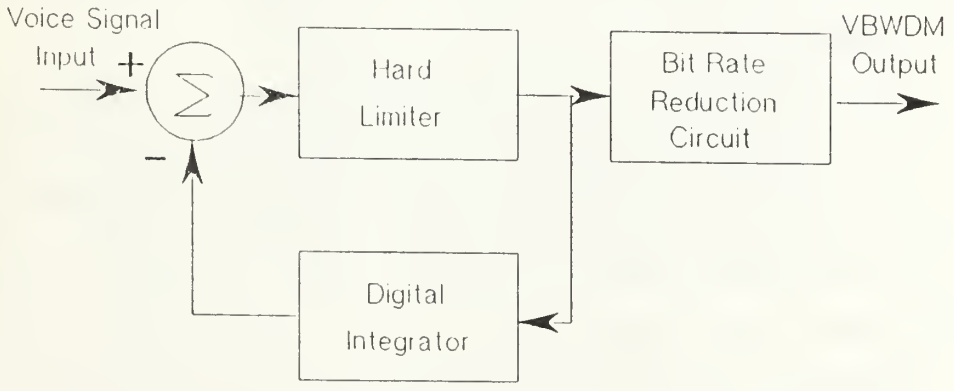


Figure 5. Block diagram of the VBWDM with the bit rate reduction circuit.

III. HARDWARE REALIZATION OF THE VBWDM

This chapter mainly deals with the explanation of the hardware blocks of the variable bit width delta modulation (VBWDM) voice communication system that has been designed, constructed and developed as a part of this research. The system consists of three parts: a transmitter, a filter which simulates a transmission channel and a receiver.

A. TRANSMITTER SUBSYSTEM

Since no carrier modulation occurs at the transmitter, there exists only an analog-to-digital (A-to-D) converter, which is the VBWDM here. The block diagram of the VBWDM transmitter is illustrated in Figure 6.

For analysis purposes, the transmitter design can be divided into three subsystems. The first two form a closed loop. These three are: the forward path, including the one bit (A-to-D) converter element of the VBWDM; the feedback path, containing the digital-to-analog (D-to-A) conversion elements that constitute the digital integrator; and the bit rate reduction circuit that follows the forward path.

The VBWDM is a hybrid design consisting of 7 linear and 3 digital integrated circuits. The complete circuit diagram is included in the Appendix. The rest of this chapter gives a detailed description of the elements that constitute the forward path, feedback path and the bit rate reduction circuit, and also explains the theory behind their operation.

1. Forward Path

Elements of the forward path are: the input amplifier, the differential amplifier and the hard limiter.

a. Input Amplifier

The input amplifier is a basic inverting amplifier design using an LF 356 op amp. Its primary function is to amplify the input signal coming from the source (signal generator or tape recorder). A secondary function is to act as a high impedance input stage to avoid loading the source. The amplitude gain (G) of the amplifier is adjusted to a desired value between one and ten by the gain control potentiometer to make the analog input voltage swing compatible with the tracking range of the feedback loop.

Special care must be taken when setting the value of G since the gain factor of the forward path affects the overall performance of the modulator. A small value of G tends to increase the average bit rate. This situation is very common in all delta

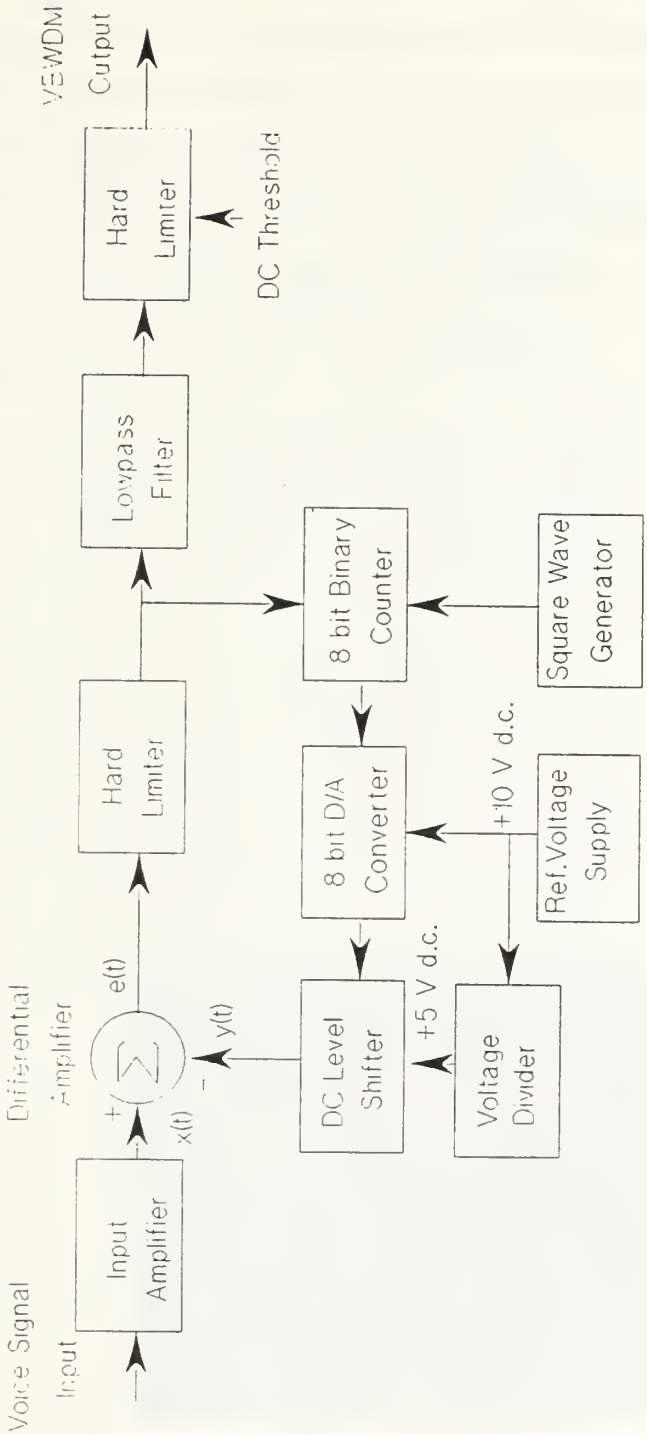


Figure 6. Block diagram of the VBWDM transmitter subsystem

modulators, and these bits are usually referred as "granular noise". In our design, granular noise occurs because the binary up/down counter is configured such that it is either counting up or down, never residing at a constant value. The continuous change at the 8-bit count vector that appears at the output of the counter, which is directly sent to the digital-to-analog converter (DAC), causes a corresponding change in the output waveform y(t) of the DAC. The voltage y(t) is the stepwise approximation of the input signal x(t). When the amplitude and sign change of y(t) exceeds that of x(t), granular noise occurs. This situation is also very commonly observed in closed loop control systems and is referred to as "hunting" which is a small amount of oscillation, usually minimized but never avoided.

Too large a value of G causes overloading of the system whereby the feedback loop exceeds its tracking limits. The cause of this situation can be explained as follows. Occasionally, the output of the hard limiter remains at either a high or low state long enough for the up/down counter to reach its highest or lowest count (binary 1111 1111 and 0000 0000 respectively) and starts counting again. This causes a discontinuity in the output waveform, y(t), of the DAC where the trace of the input waveform x(t) is temporarily lost and an ambiguous situation is met. Figure 7 illustrates this situation. This is another natural behavior of the design. To avoid this situation, G should be adjusted such that the amplitude swing at the output of the amplifier x(t) is kept between +5 and -5 volts.



Figure 7. Discontinuity of y(t) due to large x(t).

b. Summing Junction

The second element of the forward path is a differential amplifier (LF 356) with inputs equally weighted. In this configuration the signal appearing at the output is the difference between the signal generated at the feedback loop, y(t), and the amplified input signal, x(t), applied to the inverting and non-inverting inputs of the opamp respectively. The output of the differential amplifier is an analog waveform referred to as the error signal, e(t), that equals to the difference between the input signals, x(t) and y(t).

c. Hard Limiter

The hard limiter is the two-level quantizer of the DM, or it can also be considered as a one-bit ADC. This circuit produces an output which is either high or low (+5 V and 0 V respectively, depending on the polarity of the signal e(t) present at its input). The hard limiter consists of an LM 311 comparator IC which produces TTL compatible output voltages.

2. Feedback Path

The feedback path of the VBWDM contains the necessary elements to regenerate the input signal, x(t), from the digitized error signal, e(t). The feedback path is referred to as the digital integrator of the VBWDM. Since x(t) is an analog waveform, to make a comparison, it is necessary to produce an analog waveform from e(t), which involves mainly a digital-to-analog conversion process. We name the resultant waveform as y(t), which is a staircase approximation to the x(t). The slope sign of y(t) is determined by the polarity of e(t).

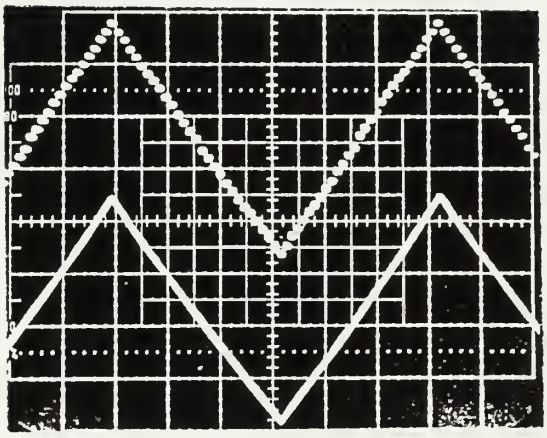
Figure 8(a) shows as the upper trace y(t) for a triangular input signal and x(t) as the lower trace. Figure 8(b) shows the same waveforms for a voice signal.

The elements of the feedback path are: an 8 bit binary up/down counter, an 8-bit digital-to-analog converter, a square-wave generator which serves as a clock, a reference voltage supply and a dc level shifter.

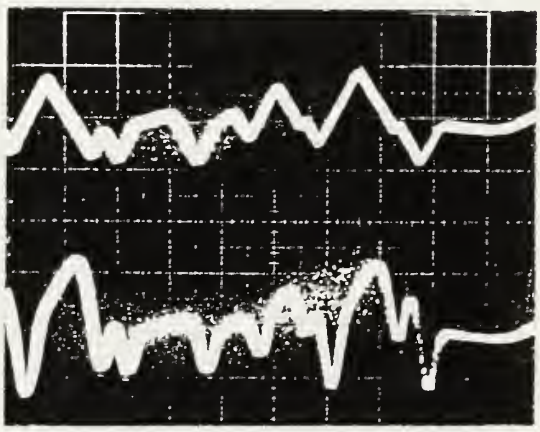
a. 8 Bit Binary Up/Down Counter

The error signal e(t) contains the slope information of the message x(t). To convert this one bit, two-level quantity into an 8-bit number, an 8-bit binary up/down counter is used.

The up/down control input of the counter is connected to the output of the hard limiter so that, when this output is in a high state (5 V or binary one), the counter counts up, and when in a low state (0 V or binary zero), the counter counts down. This



(a) Triangular wave input.



(b) Voice signal input.

Figure 8. Staircase approximations (upper trace) for inputs (lower trace).

way, an 8-bit binary count vector is produced at the output of the counter, that corresponds to the integral of e(t).

Hardware realization of this 8-bit counter is done by cascading two 4-bit binary counter ICs (CD 4029), where the first one produces the lower 4-bits and the second one produces the higher 4 bits of the count vector. Upon reaching an all-one state (1111 binary), the first counter chip issues a "carry out" for the second one, which enables it to proceed counting. The 8-bit parallel output of the counter is connected to the inputs of the 8-bit DAC with the same order.

b. 8 Bit Digital-to-Analog Converter

The DAC converts the 8-bit count vector to a corresponding analog quantity. Depending on the binary count value, an analog voltage between 0 V and 10 V is produced at the output of the DAC, where binary 0000 0000 corresponds to 0 V and binary 1111 1111 corresponds to 10 V. In this case, the step size is 40 millivolts. Continuous change of the count value leads to a continuous change of the output. The resultant waveform y(t) is a staircase approximation to x(t).

Hardware realization of the DAC is done by using a DAC 0807 IC, which has TTL-and CMOS-compatible noninverting inputs and does not require a clock pulse to perform conversion.

c. DC Level Shifter

As stated above, the output, y(t), of the DAC is an analog waveform whose amplitude varies between 0 V to 10 V. To make the comparison with the input waveform, x(t), which has no dc component, it is necessary to apply a dc level shift to y(t). This is done simply by adding -5 V to y(t), where 5 V is obtained by a resistive voltage divider from the 10 V reference voltage supply.

Hardware realization of the dc level shifter is a basic differential amplifier application with LF 356 opamp, where 5 V is applied to the inverting input and the DAC ouput is applied to the non-inverting input. The resistance values are chosen to give a unity gain to the differential amplifier.

d. Square Wave Generator

A TTL compatible square pulse is required for the counter chips. A voltage-controlled oscillator (VCO) chip, ICL 8038, with square wave output is used for this purpose. The VCO is configured to give a 50% duty cycle waveform. The dc frequency control voltage to the VCO is supplied via a potentiometer and the output frequency f_g is adjusted by this potentiometer.

The output frequency f_s determines the slew rate of the feedback path. It does this by directly controlling the counting speed of the counter chips. If f_s is too small, y(t) falls behind x(t) and a slope overload condition occurs. If f_s is too large, granular noise is created. With f_s in the range 60 kHz to 140 kHz, the modulator worked satisfactorily. A value of $f_s = 110$ kHz gave the best result for voice and music signals. At this frequency, the slew rate of the feedback loop is calculated as 3.5 V/msec, which enables it to follow a 2 V_{pp} sinusoid at 1.7 kHz or, equivalently, a 4 V_{pp} sinusoid at 850 Hz. Figure 9 illustrates the slope overload due to a value of f_s equal to 40 kHz with a 1 kHz sinusoidal input signal where $V_{pp} = 2$ V.

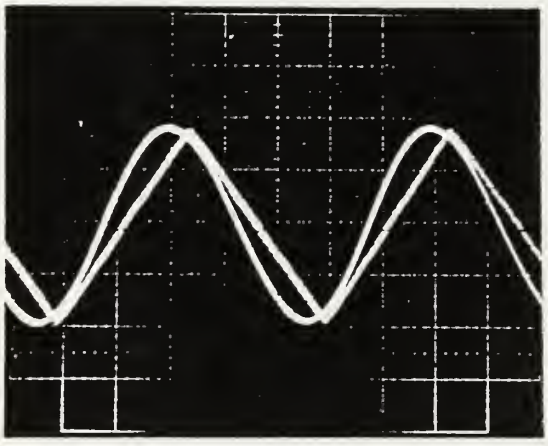


Figure 9. Slope overload due to a small value of generator frequency f_s (0.5 V/div, 0.2msec/div).

e. Reference Voltage Supply

For proper functioning of the DAC 0807, a 10.0 V reference voltage is required. An adjustable voltage supply was built to reduce and regulate the 15 V board supply voltage to 10.0 V by using an LM 317 voltage regulator IC.

3. Bit-Rate Reduction Circuit

As mentioned earlier, DM systems generally suffer from two major problems, slope overload and granular noise. In usual applications, slope overload is reduced by increasing the clock rate or by reducing the step size, or both. In this application, since the step size was fixed (40 millivolts), the problem is solved by increasing the value of f_s. In this application, to avoid granular noise, we applied filtering at the transmitter.

Since no synchronization pulses were sent, this filtering process did not introduce any problems.

The pictures in Figure 10 illustrate how well the bit-rate reduction circuit removes the granular noise. In Figure 10(a) the triangular input signal (lower trace) to the VBWDM, and the corresponding bit stream (upper trace) at the input of the bit-rate reduction circuit is shown. It is seen that granular noise exists at the regions where an instant slope change at the input signal occurs. In Figure 10(b) the picture shows the output of the bit-rate reduction circuit (upper trace) with respect to the same input (lower trace). It is seen that the granular noise bits are removed successfully.

The bit-rate reduction circuit, which is the final block of the transmitter subsystem, has two elements, a lowpass filter (LPF) followed by a comparator with adjustable dc threshold.

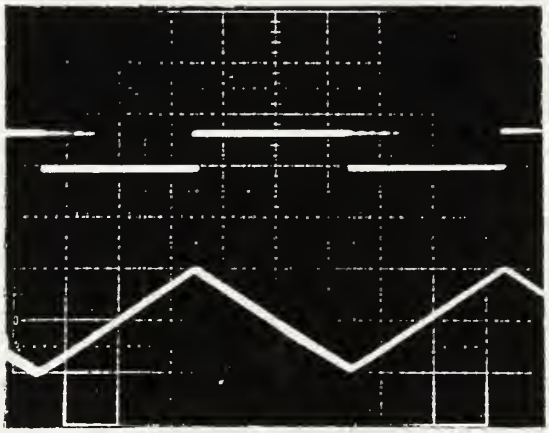
a. Lowpass Filter

When no signal is present at the input of the modulator, a pulse train from the hard limiter at half the frequency f_g of the generator (55 kHz in this case) appears at the input of the LPF. The goal is to prevent these pulses from reaching the communication channel, since they increase the average bit rate and contain no information. With this reasoning, it is obvious that the cutoff frequency (f_c) of the LPF should be chosen to be less than 55 kHz. But f_c should have value large enough to pass the pulses that contain the information during the normal operation of the modulator. The filter cutoff frequency f_c is experimentally selected as 10 kHz. An AF 150 second-order active filter IC is used to realize the LPF. The LPF also removes the high frequency components introduced by the hard limiting process.

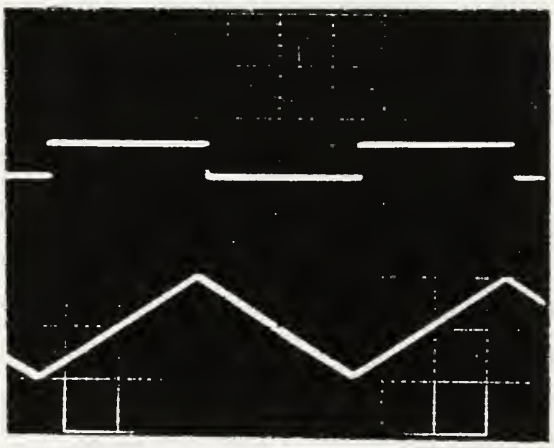
b. Hard Limiter

The output waveform of the LPF is analog. For this reason another hard limiter is used at this stage as an A-to-D converter. The hard limiter was built using an LM 311 comparator IC.

The only difference between this hard limiter stage and the one realized in the DM is that this one has an adjustable dc threshold. The output of the first hard limiter is unipolar and the LPF is dc-coupled to it. Therefore, the waveform at the input of the second hard limiter, which is the output of the LPF, contains a dc component. From the measurements taken at the input of the hard limiter, this dc component was found to be lower than 0.5 V at all times; therefore, the threshold voltage is adjusted to this value to assure the proper functioning of the hard limiter.



(a) The input bit stream (upper trace).



(b) The output bit stream (upper trace).

Figure 10. The input and the output of the bit rate reduction circuit that correspond to the triangular waveform applied to the VBWDM.

The output waveform of the hard limiter is again in TTL- compatible digital form. In carrier systems, these pulses are sent to a carrier modulator before passing through the communication channel. In our application no carrier modulation is used and so the pulses are sent directly to the communication channel which is simulated with a LPF.

B. CHANNEL SIMULATING FILTER

One of the main objectives of this research is to determine the channel bandwidth (BW) required for intelligible voice communication with VBWDM, since most practical communications applications are through bandlimited channels.

In usual DM applications, the bit rate is equivalent to the clock rate of the modulator. In our case, there is no clock used at the modulator, therefore neither the number of bits transmitted to the channel nor the bit width (bit period) is a constant value. For these reasons, it is not possible to calculate the required BW analytically. The experimental procedure used for determining the BW requirement is as follows. Since only pulses (baseband signal) are sent, a LPF is the appropriate choice to simulate the bandlimited communication channel. The criteria used for determining the cutoff frequency of the LPF is based on intelligibility of the recovered message at the receiver output, which is the voice signal reproduced by the speaker. By trial, the BW required is determined as 1.5 kHz for intelligible voice transmission.

An AF 150 LPF IC is used for the hardware realization of the channel filter. The picture in Figure 11 illustrates the behavior of the channel filter to the transmitted pulses. The measured frequency response of the filter is given in Figure 12 and the circuit diagram is included in the Appendix.



Figure 11. The input pulse train to the channel filter (upper trace) and the output (lower trace).

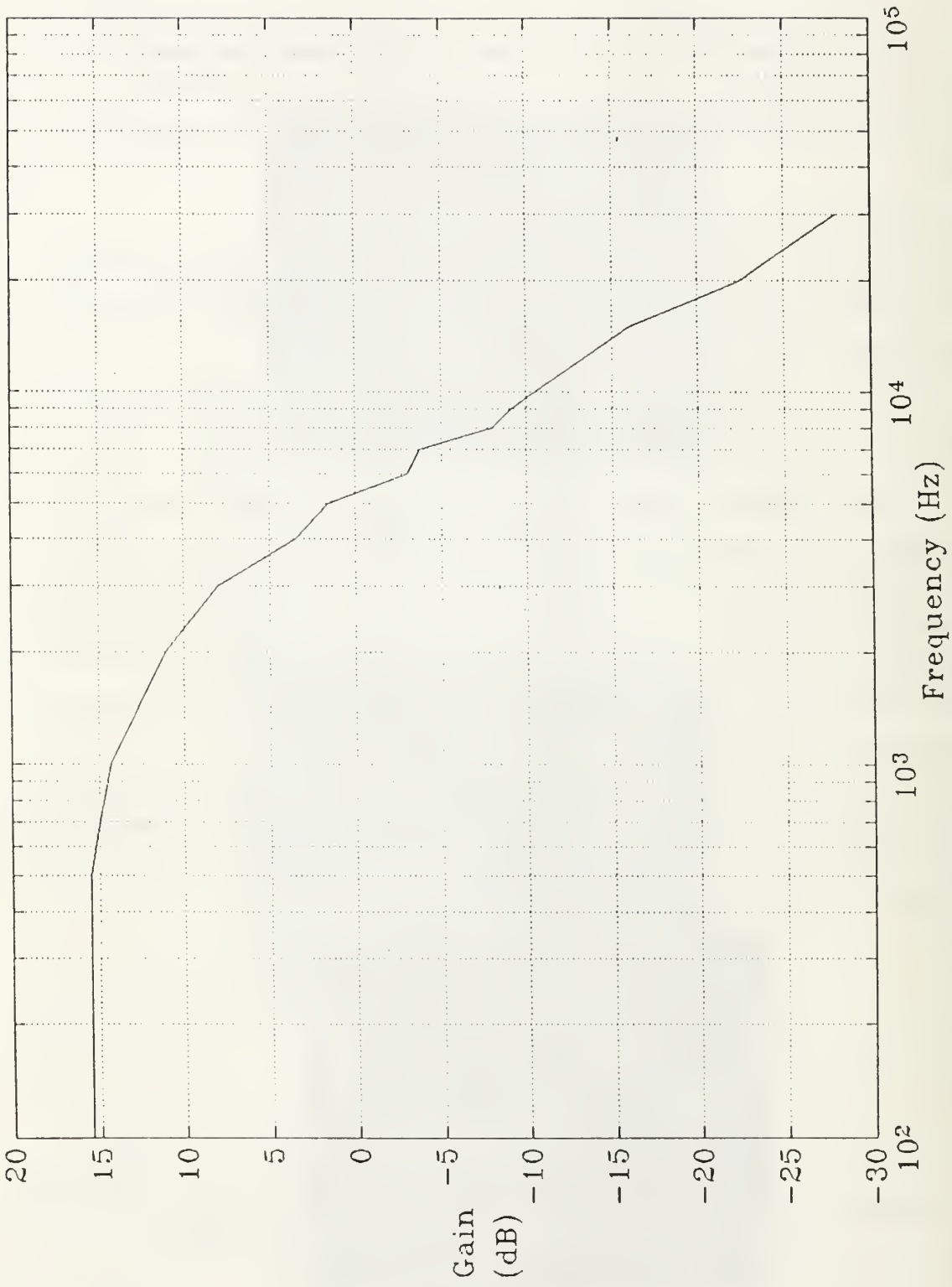


Figure 12. Frequency response of the channel simulating LPF.

C. RECEIVER SUBSYSTEM

The usual demodulator for a DM application is the replica of the feedback loop that is used in the modulator. In this application, our goal was to reproduce an intelligible voice signal from the output of the channel in a simple way.

As seen in Figure 13, the receiver consists of a lowpass filter and an audio amplifier. The circuit diagram is included in the Appendix.

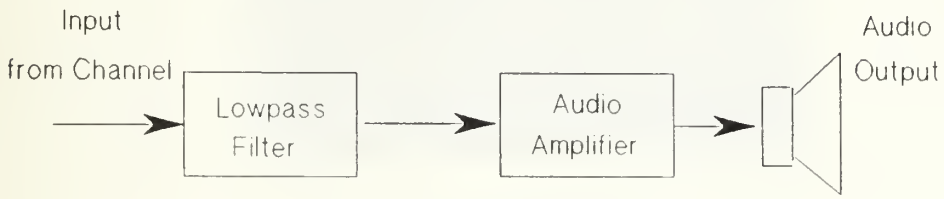


Figure 13. Block diagram of the receiver subsystem.

1. Receiver Filter

The LPF used here corresponds to the "leaky integrator" or to the "accumulator" used in the demodulator part of the usual DM applications. It has a second-order transfer function and a 3 dB cutoff frequency of 1.5 kHz.

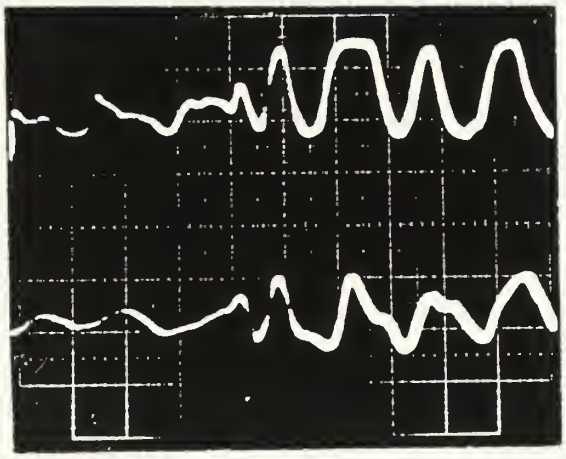
The channel filter and the receiver filter have the same properties and, when cascaded (as in our application) they form a LPF of fourth-order whose 3 dB cutoff frequency is 1 kHz, with a 40 db per decade attenuation slope thereafter. Due to the gain characteristics of the AF 150 IC, a total gain factor of between 31 db to 16 db (values are for 100 Hz and 3 kHz respectively) is applied to the signal after the modulator.

2. Audio Amplifier

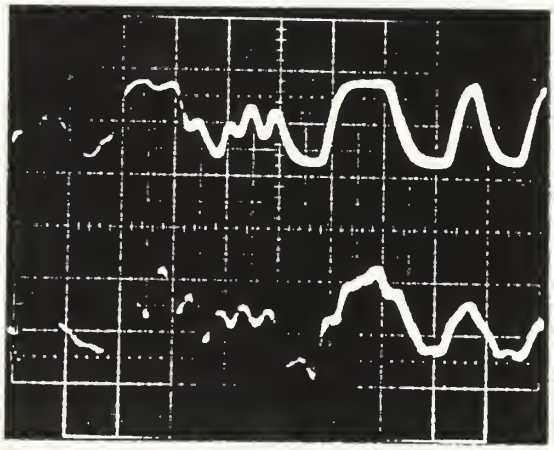
To drive a loudspeaker for reproduction of voice signals, an audio amplifier was used after the LPF. By using the volume adjust potentiometer, the gain of the amplifier

is adjusted to a desired level between 0 db and 20 db. The hardware realization of the audio amplifier uses an LM 318N IC.

The photographs in Figure 14 illustrate three sample input signals to the VBWDM and their corresponding reproduced forms at the receiver output.



(a) Voice signal.



(b) Music signal.

Figure 14. Sample input signals to the VBWDM (lower traces) and their reproduced forms at the receiver (upper traces).

IV. HARDWARE REALIZATION OF THE HARD LIMITER TYPE OF ADC

This chapter gives the detailed description of the hardware and the operation of the hard limiter type of analog-to-digital converter (ADC) that was designed, built and tested as a part of this research.

It is well-known that hard limited voice signals are intelligible when recovered with a speaker (LPF). However, the absence of a signal at the input of the hard limiter or the presence of a weak voice signal creates rapid switching of the limiter output. This results in high average bit rates. In the design of the open-loop ADC here, a circuit is included to prevent this rapid switching.

A. ONE-BIT ADC

The system is an open-loop system, and the decision criteria of the one-bit A-to-D conversion process is mainly based upon comparison of the analog input waveform with a constant dc threshold voltage setting.

In the hardware realization, 1 logic and 8 linear ICs are used. The complete circuit diagram of the hard limiter type of ADC is included in the Appendix.

The block diagram of the one-bit hard limiter type of ADC design is shown in Figure 15. The design is divided into three functional parts: the switch control circuit, the hard limiter and the TTL output stage.

1. Switch Control Circuit

The purpose of the circuit is to provide the control voltage for the analog switch IC (CD 4066) to make it close when the magnitude of the input signal is above the threshold level and to make it open otherwise. The switch control circuit consists of an absolute value amplifier and a comparator with dc threshold setting.

a. Absolute Value Amplifier

Two LM 301 op amps are used for the hardware realization. The circuit actually is an inverting type. Therefore, a unity gain inverter stage with another LM 301 op amp follows the absolute value amplifier.

The purpose of the circuit is to transform the input signal into a unipolar form. This is required for making it possible to use a single threshold setting for bipolar (analog) input signals (voice, music signal from a tape recorder or a test signal from a signal generator).

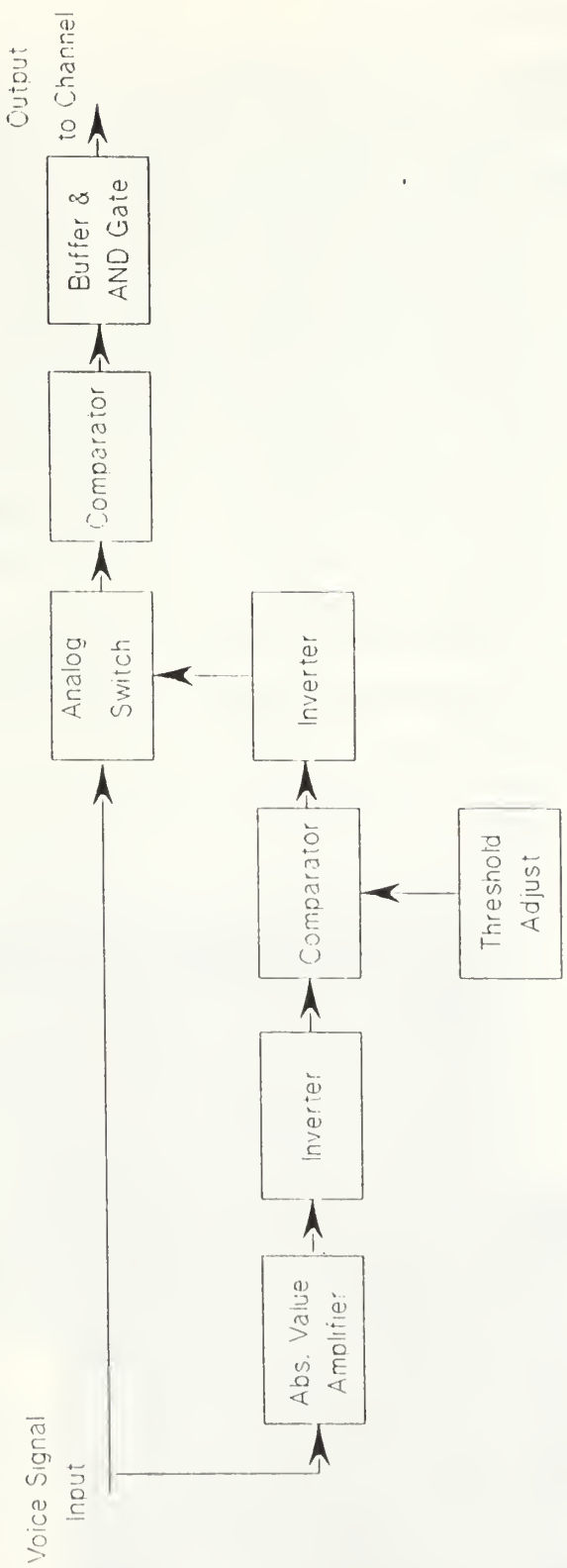


Figure 15. Block diagram of the hard limiter type of ADC.

b. Comparator with Threshold

The comparator is constructed using an LF 356 op amp. The inverting input is connected to the output of the absolute value amplifier and the noninverting input is connected to a potentiometer that acts as a resistive voltage divider for the dc threshold setting. In relation to this dc threshold level, if the absolute value of the input signal is above this level, a -15 volt output occurs. Otherwise, +15 volts is generated at the output of the comparator. The comparator output is the analog switch control voltage. Due to the specifications of the CD 4066 analog switch IC, the control voltage is required to be a unipolar quantity. (it requires 0 volts for the switch to open and +15 volts to close). Rectification with a diode (1N4148) and inversion (with a unity-gain inverter that uses an LM 356 op amp) is applied to the output voltage of the comparator to meet these specifications.

2. Hard Limiter Stage

The hard limiter stage contains the elements that perform the one-bit (two-level) A-to-D conversion. These are the analog switch and the comparator.

a. Analog Switch

A CD 4066 chip is used as the analog switch. The analog input signal is connected to the input terminal, and the output of the switch control circuit is applied to the control terminal. With this configuration, only the parts of the signal that exceeds the specified threshold value are passed to the comparator. The portion of the signal in the region about zero volts is removed so as to reduce the bit rate (remove rapid switching effects). The photograph in Figure 16 illustrates the analog waveform (voice waveform) at the input of the switch (upper trace), and the corresponding switch output (lower trace), where the small amplitude (unvoiced parts) of the speech signal are removed.

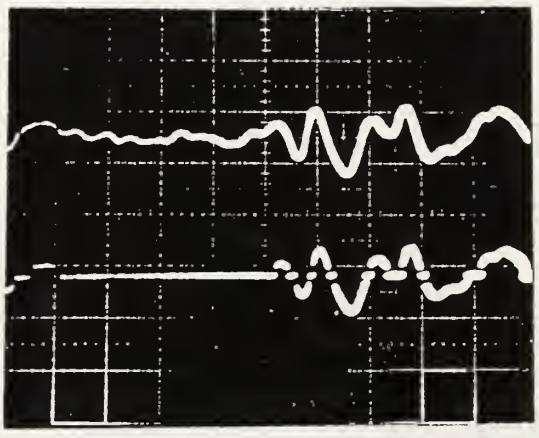


Figure 16. Removal of the unvoiced parts from the speech signal.

b. Comparator

The comparator is the one-bit (two-level) ADC. The circuit consists of an LF 356 op amp. The non-inverting input is connected to ground as a reference and the inverting input to the output of the analog switch. When the waveform received from the analog switch is above ground potential, the comparator output is -15 volts. When the analog switch is open or the waveform is below ground potential, +15 volts occur at the output. As the remaining part of the circuit is designed for unipolar operation, half-wave rectification of the comparator output is performed using a 1N4148 diode. After rectification, the amplitude of the voltage is adjusted by using a potentiometer to give +5V maximum output.

3. TTL Output Stage

This circuit converts the bit stream generated by the hard limiter to a TTL-compatible unipolar return-to-zero (RZ) format. The elements of this stage are a voltage follower and an AND gate.

The picture in Figure 17 shows a voice signal at the input of the comparator and the corresponding RZ waveform achieved at the output of the TTL output stage, which is also the output of the hard limiter type of ADC.

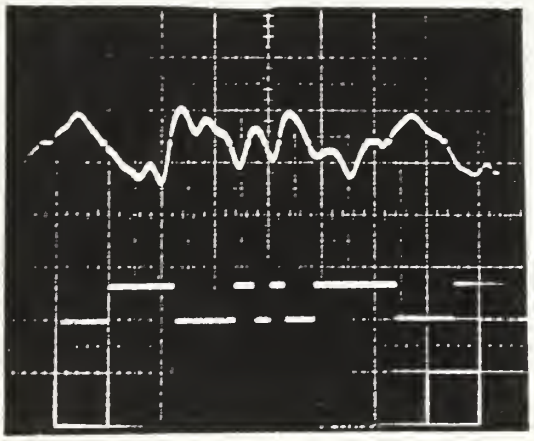


Figure 17. Voice signal and the corresponding bit stream at the output of the hard limiter type of ADC.

a. Voltage Follower

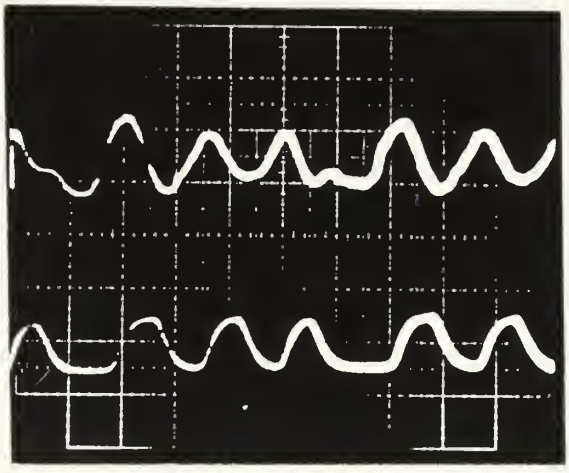
An LM 310 voltage follower IC is used for this purpose. This is the intermediate stage between the comparator and the AND gate. It acts as a buffer for the comparator to drive the TTL AND gate.

b. AND Gate

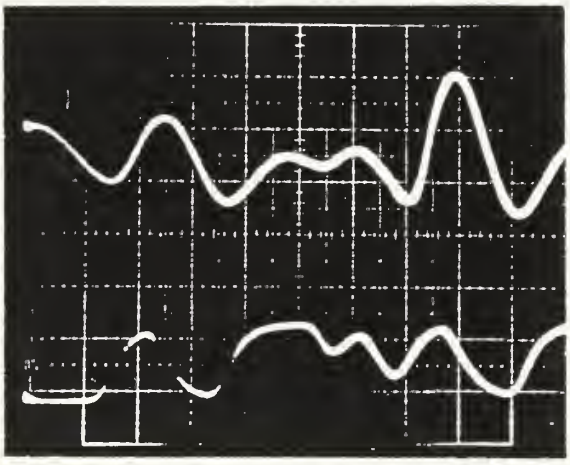
To give the waveform a TTL compatible shape, an AND gate is used at the output stage. One input of the AND gate is connected to +5 volts and the other input to the output of the voltage follower. In this configuration the AND gate produces a "0" for input voltages less than 0.8 volts and a "1" for inputs larger than 2 volts. These outputs correspond to 0.2 volts and 3.4 volts respectively for a typical 7408 (TTL) IC.

The remaining parts of the system, the channel filter and the receiver, are the same as described in the previous chapter.

The photographs in Figure 18 illustrate two sample input signals to the hard limiter type of ADC and their corresponding reproduced forms at the receiver output.



(a) Music signal.



(b) Voice signal.

Figure 18. Sample input signals to hard limiter type of ADC (upper traces) and their reproduced forms at the receiver (lower traces).

V. MEASUREMENTS AND RESULTS

Since the bits entering the channel filter have variable widths, the bit rate is not constant. Consequently, the average bit rate is measured as follows. A frequency counter counts for one second the number of binary one bits entering the channel, and the largest number displayed on the counter during a speech passage of several seconds is recorded. The number of binary zeros in that passage equals to the number of ones, since for each high level of voltage there has to follow a low level. So, the average bit rate is twice the counter reading.

Applying this method, the average bit rate is determined to be in the range of 2 to 4 kbps for voice and 2 to 5 kbps for music signals, using VBWDM. For the hard limiter type of ADC, the results are 1 to 3 kbps and 1 to 4 kbps, respectively.

It is observed that bit rate is dependent on the vocal characteristics and the sex of the speaker. Also the quality and the intelligibility achieved with the VBWDM is found to be better than the hard limiter type of ADC for the same average bit rate.

Determination of the minimum bandwidth requirement is done by decreasing the 3 dB cutoff frequency of the channel filter. The decision criteria was again the intelligibility of the reproduced signal. At each trial, the same sample messages are used for evaluation. With this method the minimum channel bandwidth is determined to be 1.5 kHz. At lower bandwidths (i.e., 1 kHz, 0.5 kHz) intelligibility is preserved to some extent, but there is a lack of speaker identification.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

A VBWDM and a hard limiter type of one-bit ADC were designed, constructed and tested in this research. The objective was to digitize the voice and music signals for communication purposes without use of a system clock (sampling at a fixed rate), so as to reduce the average bit rate and the occupied channel bandwidth that is required for transmission of binary audio. This objective is met with both designs, and intelligible voice transmission is achieved at low bit rates without requiring synchronization. Also it is observed that the communication link realized is robust to channel degradation.

Another favorable feature of the design besides the hardware simplicity is that no transmission occurs when the signal is absent at the input of the modulator, which means a saving in the transmitter power. This is a desired feature, especially for mobile stations where power sources are limited.

Since the design does not require synchronization or framing of bits, no continuous transmission is necessary. In military applications this feature will reduce the probability of being intercepted by hostile sources.

Disadvantages of an unclocked system are a lack of multiplexing capability and inability to apply error control coding.

The designs may be applicable in cases where limited bandwidth usage is desired or mandated, and the intelligibility is more important than the reproduction quality of the message. Examples include a service network between two stations, and a tactical emergency link in a military operation that can be used in case of failure of the other available equipment, or against broadband jamming where a small portion of the spectrum is known to be left without threat.

B. RECOMMENDATIONS

Although it will introduce hardware complexity, to improve system performance, it is suggested that the VBWDM be made adaptive by making the step size variable, or relating the oscillating frequency of the isolated generator in the feedback loop to a parameter of the input signal.

APPENDIX A. SCHEMATIC DIAGRAMS

This appendix contains the schematic (wiring) diagrams of the circuits built and operated in this research.

Figure 19 is a schematic diagram of the VBWDM. The bit rate reduction circuit schematic diagram is Figure 20. Shown next is the channel filter circuit in Figure 21.

The receiver schematic diagram is Figure 22, and the the hard limiter type of ADC schematic diagram is Figure 23.

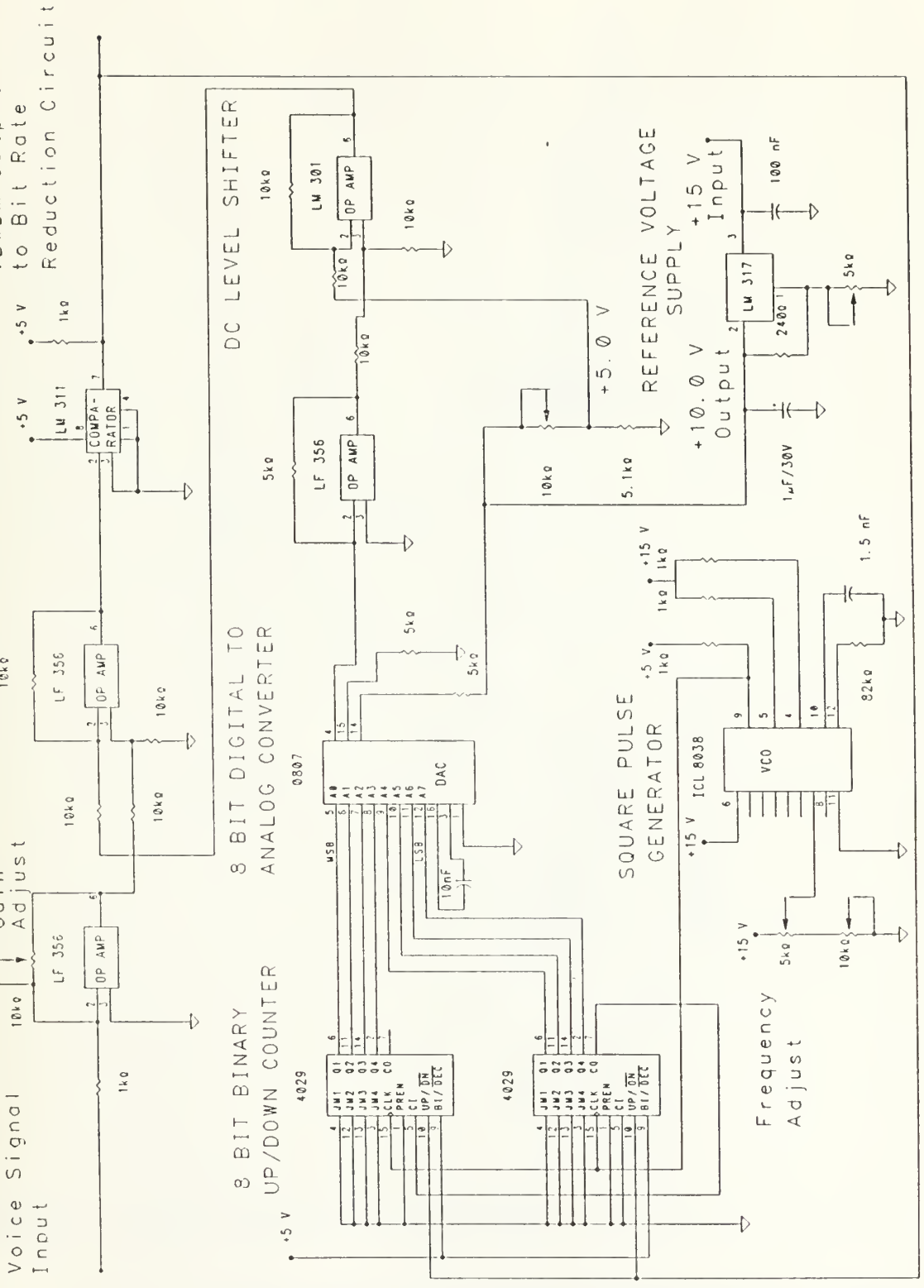


Figure 19. Schematic diagram of the VBWDM.

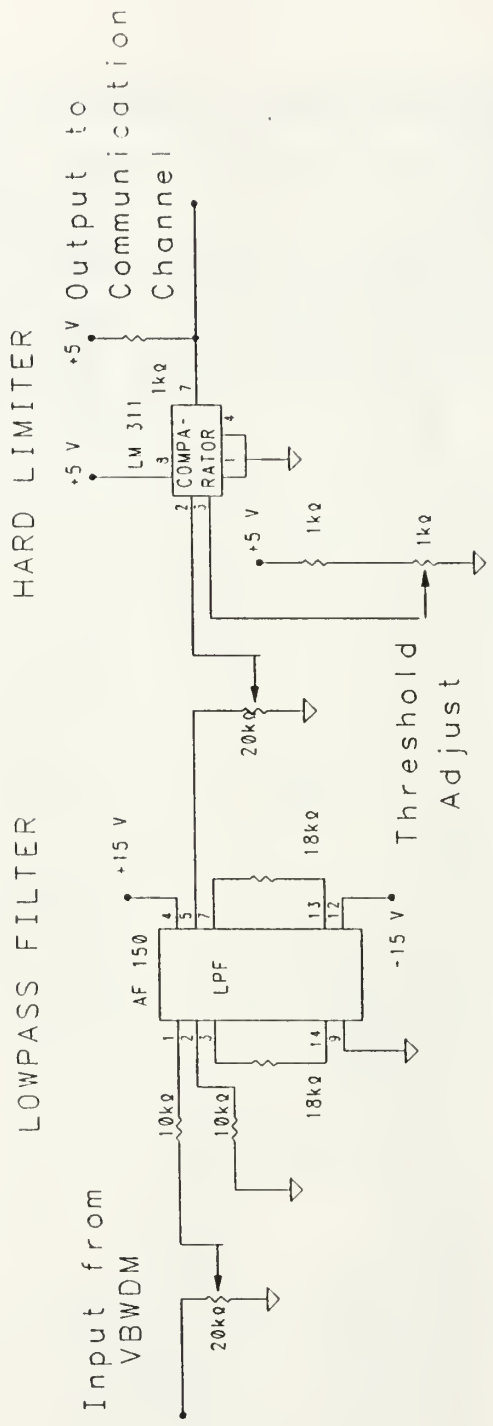


Figure 20. Schematic diagram of the bit rate reduction circuit.

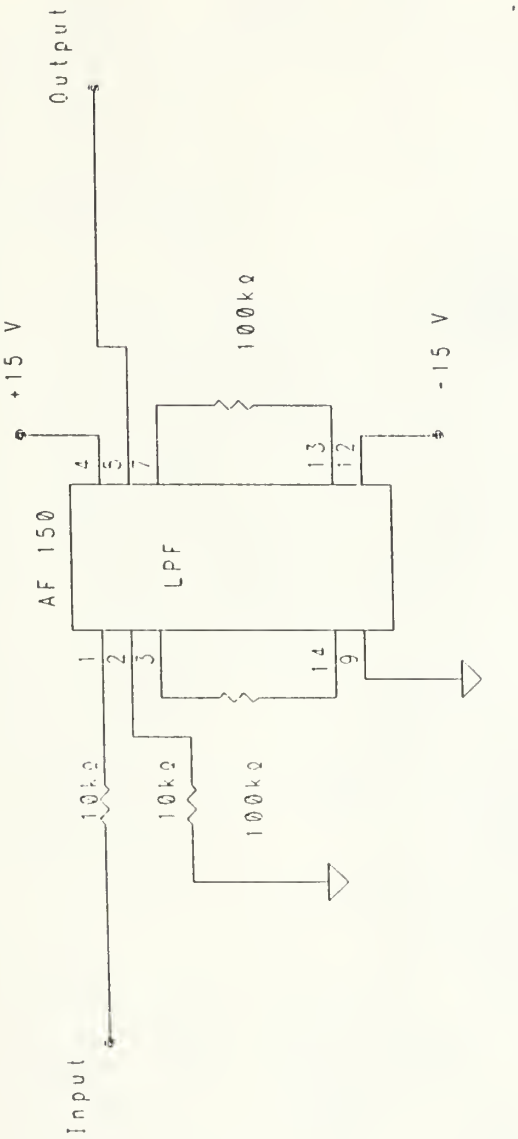


Figure 21. Schematic diagram of the channel filter.

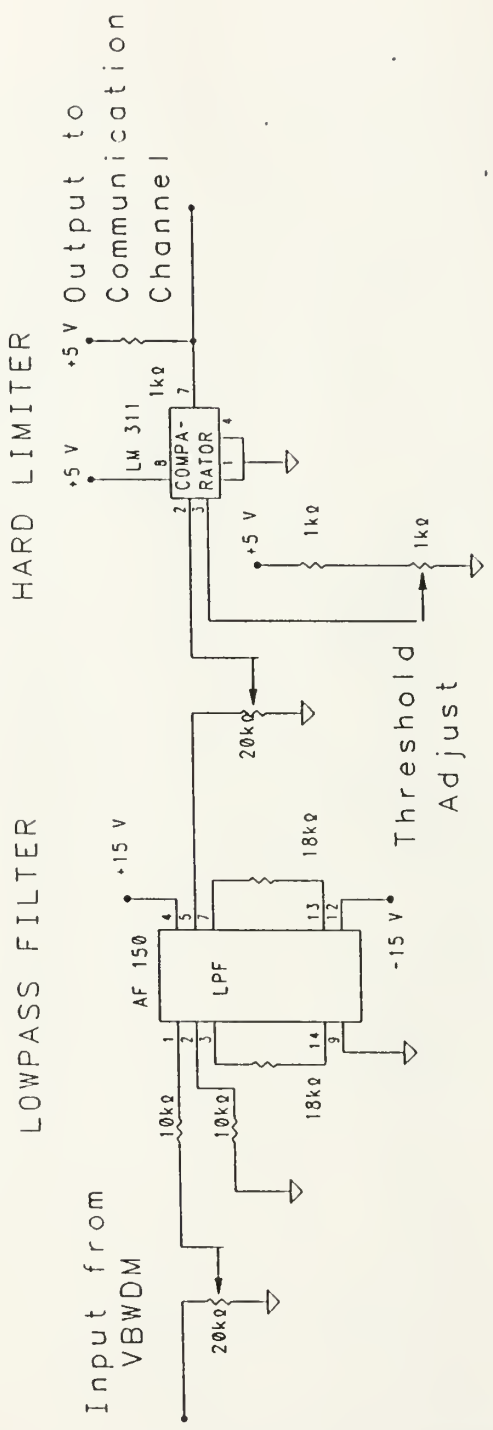


Figure 22. Schematic diagram of the receiver.

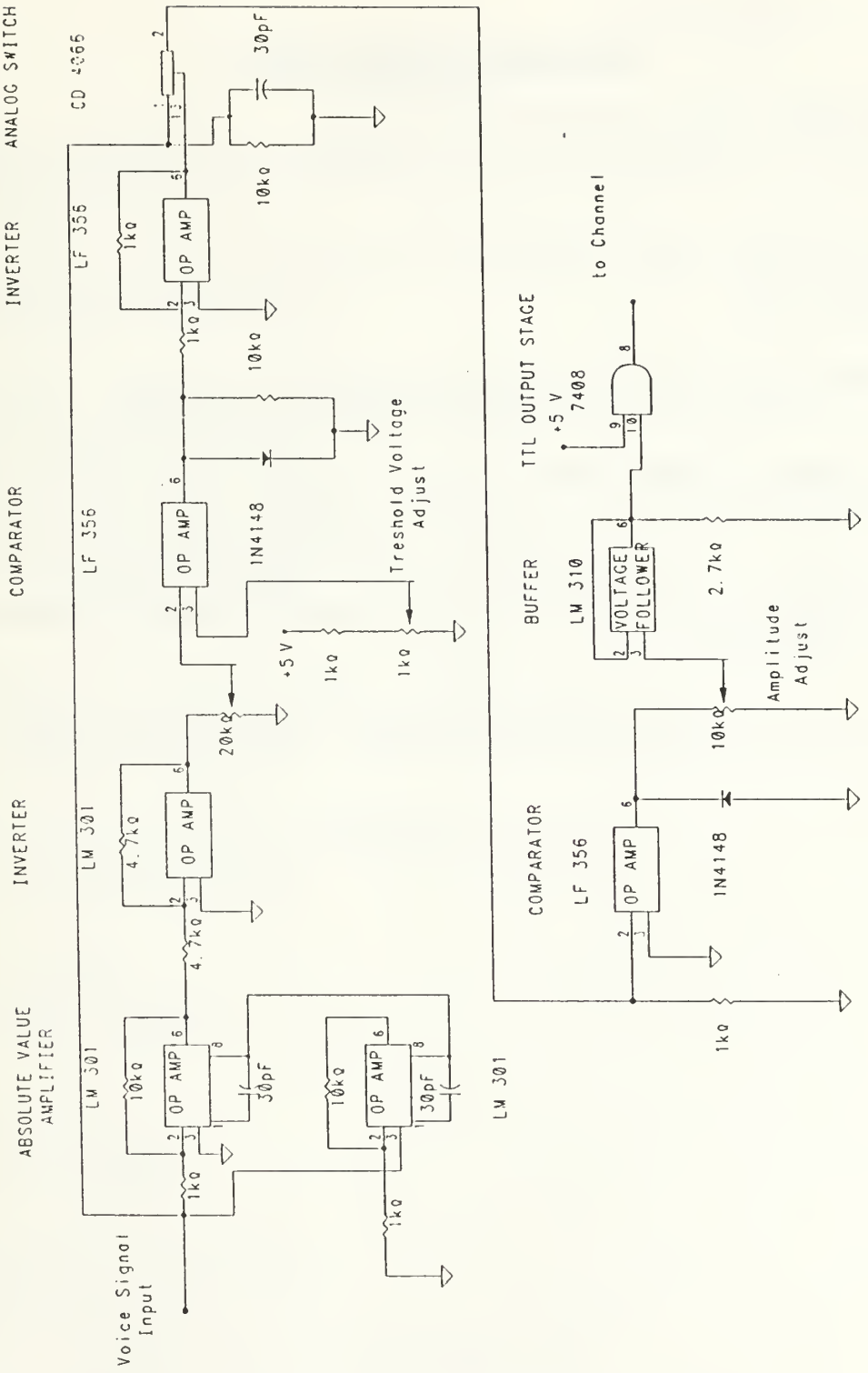


Figure 23. Schematic diagram of the hard limiter type of ADC.

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